In the Claims:

Claims 1-12 (Cancelled)

Claim 13 (Previously Presented): A method of achieving a balance between response time and system latency in a communication system, said communication system including a receiver and a transmitter, wherein sample processing is divided into time slices within said communication system, said method comprising the steps of:

employing a receive sample buffer and a transmit sample buffer, each having a first buffer size L1 capable of quick response times;

employing a receive sample buffer and a transmit sample buffer, each having a second buffer size L2 capable of accommodating system latency;

employing a switching device enabling said communication system to dynamically switch between said transmit sample buffers and between said receive sample buffers;

making a determination to switch between said first buffer size L1 and said second buffer size L2 before the activation of said transmitter during a time slice N;

processing said receive sample buffer having said first buffer size L1 and said transmit sample buffer having said first buffer size L1 during a time slice N-1;

processing said receive sample buffer having said first buffer size L1 and said transmit sample buffer having said second buffer size L2 during said time slice N;

processing said receive sample buffer having said first buffer size L1 and said transmit sample buffer having said second buffer size L2 during a time slice N+1; and

processing said receive sample buffer having said second buffer size L2 and said transmit sample buffer having said second buffer size L2 during a time slice N+2 and during time slices thereafter until deciding to switch between said first buffer size L1 and said second buffer size L2.

Claim 14 (Original): The method of claim 13, wherein the size of said transmit and receive sample buffers is coherently switched without any loss of data.

Claim 15 (Previously Presented): A system for achieving a balance between response time and system latency in a communication system, said system comprising:

sample buffers having a first buffer size capable of quick response times;

sample buffers having a second buffer size capable of accommodating system latency; and

a switching device capable of dynamically switching between the use of said sample buffers having said first buffer size and said sample buffers having said second buffer size.

Claim 16 (Original): The system of claim 15, wherein said second buffer size is robust so as to accommodate system latency.

Claim 17 (Original): The system of claim 15, wherein said sample buffers are maintained in a memory.

Claim 18 (Original): The system of claim 15, wherein said sample buffers are maintained in physical buffers.

Claim 19 (Original): The system of claim 15, wherein said dynamic switching is performed in response to communication system operating requirements.

Claim 20 (Original): The system of claim 15, wherein said system latency comprises interrupt latency.

Claim 21 (Original): The system of claim 15, wherein said system latency comprises bus latency.

Claim 22 (Original): The system of claim 15, wherein said system latency comprises both interrupt latency and bus latency.

Claim 23 (Original): The system of claim 15, wherein the size of said sample buffers is coherently switched without any loss of data.

Claim 24 (Original): The system of claim 15, wherein said second buffer size is greater than said first buffer size.

Claim 25 (Previously Presented): The system of claim 15, wherein the size of said sample buffers is switched to said first buffer size when a modem connection is reinitialized or restarted.

Claim 26 (Previously Presented): The system of claim 15, wherein the size of said sample buffers is switched to said first buffer size when a retrain sequence has been initialized, wherein said communication system implements an International Telecommunication Union standard chosen from the group of V.32, V.32bis and V.34.

Claim 27 (Previously Presented): A system for achieving a balance between response time and system latency in a communication system, said system comprising:

sample buffers having a first buffer size capable of quick response times;

sample buffers having a second buffer size that is robust so as to accommodate system latency; and

a switching device capable of dynamically switching between the use of said sample buffers having said first buffer size and said sample buffers having said second buffer size.

Claim 28 (Original): A system for achieving a balance between response time and system latency in a communication system, said system comprising:

a sample buffer that is variable in size, wherein the sample buffer has a first buffer size capable of quick response times and a second buffer size capable of accommodating system latency; and

a switching device capable of dynamically switching between said first buffer size and said second buffer size of the sample buffer.

Claim 29 (Currently Amended): A machine readable storage medium containing executable instructions which, when executed by a machine, causes the machine to perform the steps of a method for achieving a balance between response time and system latency in a communication system, the method comprising:

employing sample buffers having a first buffer size capable of quick response times;

employing sample buffers having a second buffer size capable of accommodating system latency; and

dynamically switching between the use of said sample buffers having said first buffer size and said sample buffers having said second buffer size.

Claim 30 (Original): The medium of claim 29, wherein said second buffer size is robust so as to accommodate system latency.

Claim 31 (Original): The medium of claim 29, wherein said dynamic switching is performed in response to communication system operating requirements.

Claim 32 (Original): The medium of claim 29, wherein said system latency comprises interrupt latency.

Claim 33 (Original): The medium of claim 29, wherein said system latency comprises bus latency.

Claim 34 (Original): The medium of claim 29, wherein said system latency comprises both interrupt latency and bus latency.

Claim 35 (Original): The medium of claim 29, wherein the size of said sample buffers is coherently switched without any loss of data.

Claim 36 (Original): The medium of claim 29, wherein said second buffer size is greater than said first buffer size.

Claim 37 (Previously Presented): The medium of claim 29, wherein the size of said sample buffers is switched to said first buffer size when a modem connection is reinitialized or restarted.

Claim 38 (Previously Presented): The medium of claim 29, wherein the size of said sample buffers is switched to said first buffer size when a retrain sequence has been initialized, wherein said communication system implements an International Telecommunication Union standard chosen from the group of V.32, V.32bis and V.34.

Claim 39 (Currently Amended): A machine readable storage medium containing executable instructions which, when executed by a machine, causes the machine to perform the steps of a method for achieving a balance between response time and system latency in a communication system, the method comprising:

employing sample buffers having a first buffer size capable of quick response times;

employing sample buffers having a second buffer size that is robust so as to accommodate system latency in said communication system; and

employing a switching device capable of dynamically switching between the use of said sample buffers having said first buffer size and said sample buffers having said second buffer size.

Claim 40 (Currently Amended): A machine readable storage medium containing executable instructions which, when executed by a machine, causes the machine to perform the steps of a method for achieving a balance between response time and system latency in a communication system, the method comprising:

employing a sample buffer that is variable in size, wherein said sample buffer has a first buffer size capable of quick response times and a second buffer size capable of accommodating system latency; and

employing a switching device capable of dynamically switching between said first buffer size and said second buffer size of said sample buffer.

Claim 41(Previously Presented): A method of achieving a balance between response time and system latency in a communication system, said method comprising:

employing sample buffers having a first buffer size capable of quick response times;

employing sample buffers having a second buffer size capable of accommodating system latency; and

employing a switching device capable of dynamically switching between said sample buffers having said first buffer size and said sample buffers having said second buffer size.

Claim 42 (Original): The method of claim 41, wherein said second buffer size is robust so as to accommodate system latency.

Claim 43 (Original): The method of claim 41, wherein said dynamic switching is performed in response to communication system operating requirements.

Claim 44 (Original): The method of claim 41, wherein said system latency comprises interrupt latency.

Claim 45 (Original): The method of claim 41, wherein said system latency comprises bus latency.

Claim 46 (Original): The method of claim 41, wherein said system latency comprises both interrupt latency and bus latency.

Claim 47 (Original): The method of claim 41, wherein the size of said sample buffers is coherently switched without any loss of data.

Claim 48 (Original): The method of claim 41, wherein said second buffer size is greater than said first buffer size.

Claim 49 (Previously Presented): The method of claim 41, wherein the size of said sample buffers is switched to said first buffer size when a modem connection is reinitialized or restarted.

Claim 50 (Previously Presented): The method of claim 41, wherein the size of said sample buffers is switched to said first buffer size when a retrain sequence has been initialized, wherein said communication system implements an International Telecommunication Union standard chosen from the group of V.32, V.32bis and V.34.

Claim 51(Previously Presented): A method of achieving a balance between response time and system latency in a communication system, said method comprising:

employing sample buffers having a first buffer size capable of quick response times;

employing sample buffers having a second buffer that is robust so as to accommodate system latency in said communication system; and

employing a switching device capable of dynamically switching between said sample buffers having said first buffer size and said sample buffers having said second buffer size.

Claim 52 (Previously Presented): A method of achieving a balance between response time and system latency in a communication system, said method comprising:

employing a sample buffer that is variable in size, wherein said sample buffer has a first buffer size capable of quick response times and a second buffer size capable of accommodating system latency; and

employing a switching device capable of dynamically switching between said first buffer size and said second buffer size of said sample buffer.

Claim 53 (Previously Presented): A modem capable of performing a start-up procedure with a remote device before entering a data phase for exchanging data with said remote device, said start-up procedure having a first start-up sequence and a second start-up sequence, said modem comprising:

a sample buffer having a first buffer size for use during said first start-up sequence;

a sample buffer having a second buffer size for use during said first start-up sequence, wherein said second buffer size is greater than said first buffer size; and

a switching device capable of switching from said sample buffer having said first buffer size to said sample buffers having said second buffer size based on a transition in said start-up procedure from said first start-up sequence to said second start-up sequence.

Claim 54 (Previously Presented): The modem of claim 53, wherein said modem achieves a balance between response time and system latency in a communication system by

switching from said sample buffer having said first buffer size to said sample buffers having said second buffer size.

Claim 55 (Previously Presented): The modem of claim 53, wherein said first start-up sequence is an initial start-up sequence of said start-up procedure.

Claim 56 (Previously Presented): The modem of claim 55, wherein said start-up procedure is performed according to the International Telecommunication Union V.32bis standard, and said initial start-up sequence includes the ranging phase of said V.32bis standard.

Claim 57 (Previously Presented): A method for use by a modem to perform a start-up procedure with a remote device before entering a data phase for exchanging data with said remote device, said start-up procedure having a first start-up sequence and a second start-up sequence, said method comprising:

employing a sample buffer having a first buffer size for use during said first start-up sequence;

employing a sample buffer having a second buffer size for use during said first start-up sequence, wherein said second buffer size is greater than said first buffer size; and

switching from said sample buffer having said first buffer size to said sample buffers having said second buffer size based on a transition in said start-up procedure from said first start-up sequence to said second start-up sequence.

Claim 58 (Previously Presented): The method of claim 57, wherein said switching achieves a balance between response time and system latency in a communication system.

Claim 59 (Previously Presented): The method of claim 57, wherein said first start-up sequence is an initial start-up sequence of said start-up procedure.

Claim 60 (Previously Presented): The method of claim 59, wherein said start-up procedure is performed according to the International Telecommunication Union V.32bis standard, and said initial start-up sequence includes the ranging phase of said V.32bis standard.